**Digital System design Lab CSE-308L**

**Semester:6th**



**Lab Report # 4**

**BCD to Seven Segment Decoder**

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**Section: A**

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**Lab 04**

**BCD to Seven Segment Decoder**

**Objective:**

To implement a BCD to Seven Segment Decoder on Spartan 6 board.

**Block Diagram:**

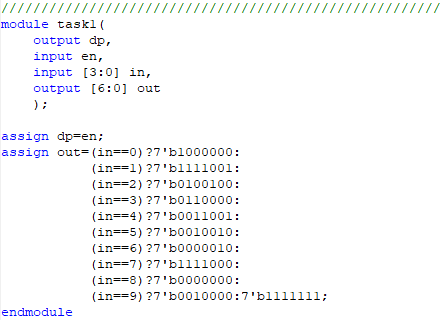
In This lab you are required to take a BCD input from the user and display that number on the seven segment display. Following diagram shows the 7 bit code for displaying “2” on the seven segment display all the input are active low signals. Note that enable signal should be held low in order to turn on the particular seven segment display. There are 4 seven segment displays on the Spartan 6 board. In later labs you will learn how to use time multiplexing techniques to turn on all the four seven segment displays as the input A,B,C,D,E,F,G, Dp are shared by all the four seven segment displays.



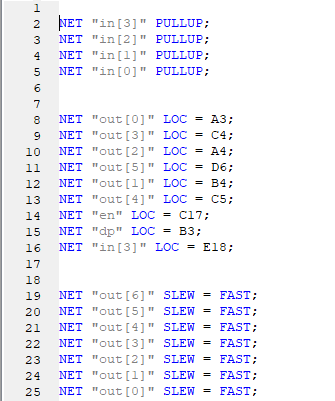
**Lab Task:**

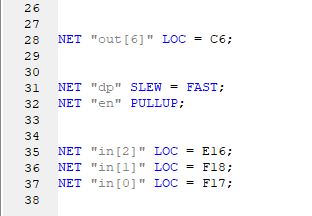
1. Using switches enter a BCD number and show the resulting number on the seven segment display.

**Code:**

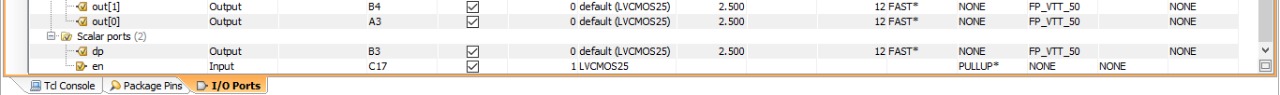
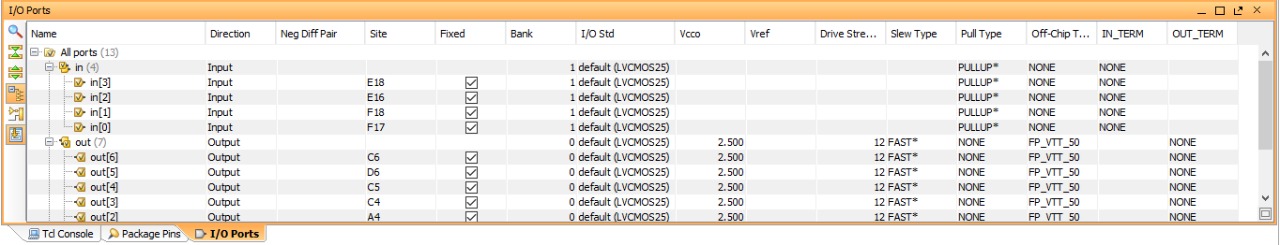


**UCF File:**

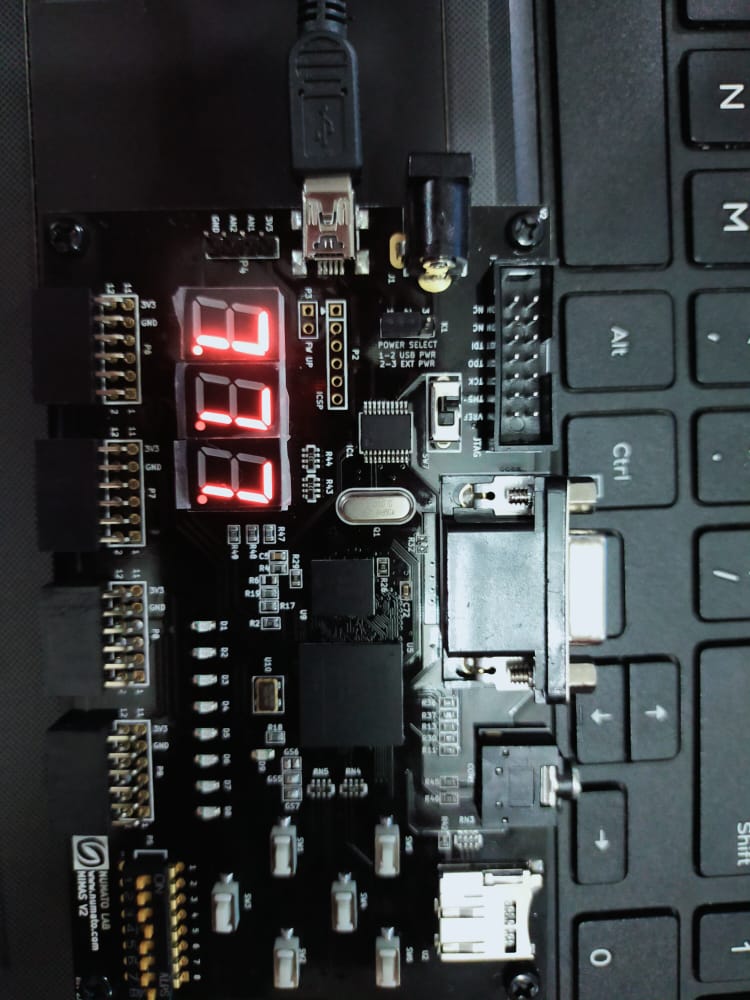


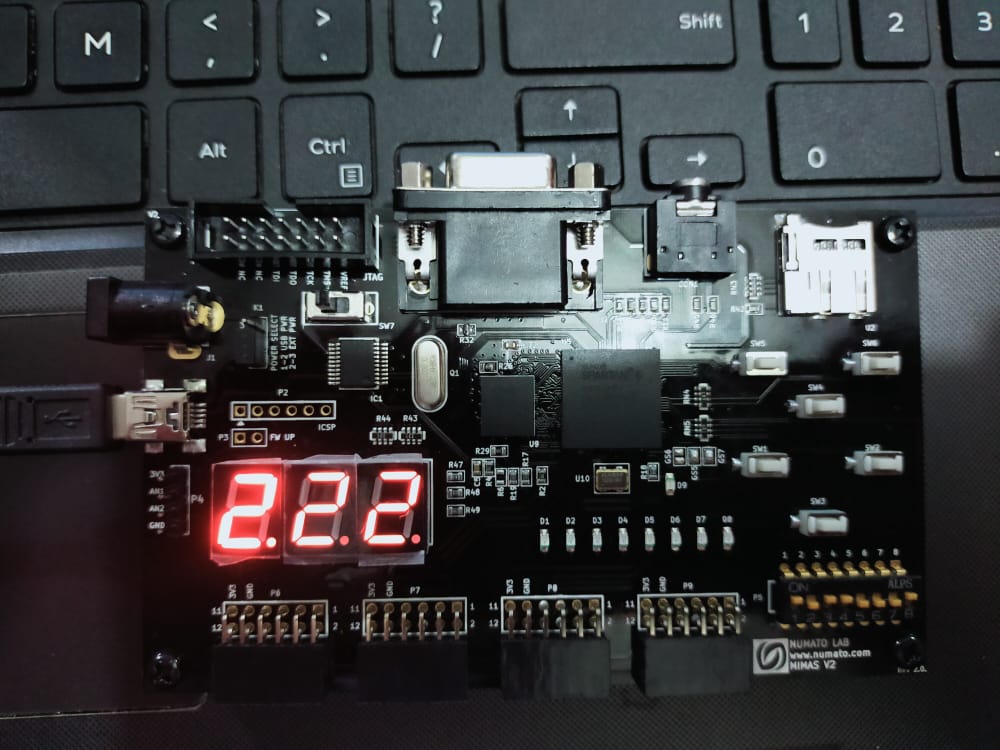


**I/O Pin Planning:**

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**Output:**

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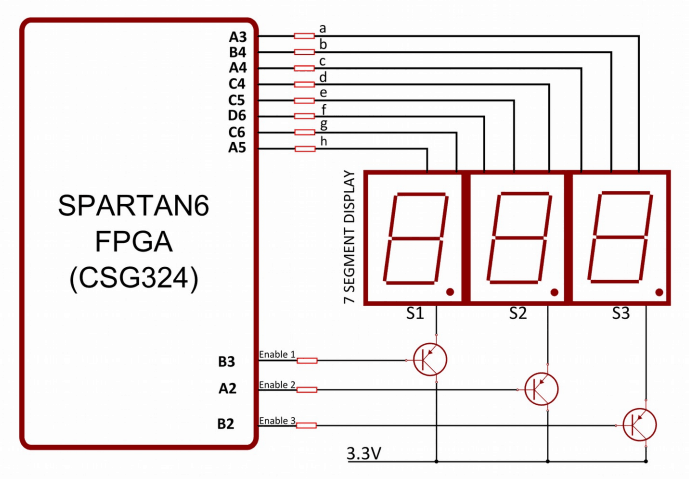
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1. Connect the output of your lab 02 (4 bit adder) to the seven segment display. Note that number above 1001 are not valid BCD numbers. In this situation keep the seven segment display off and just the dp on.

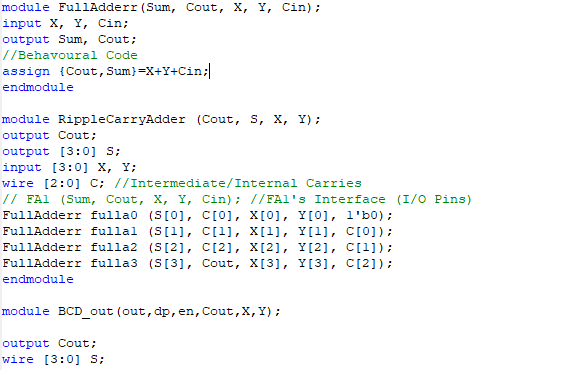
# 7 Segment Led Display On Spartan 6 Board

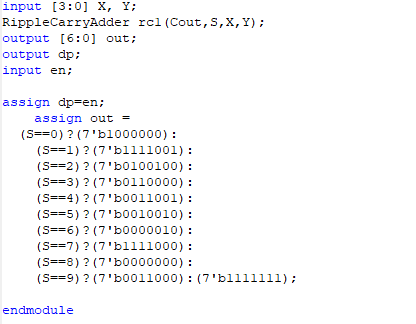
# This board features three 7-segment LED display multiplexed for low pin count operation. Each module can be separately turned on and off with the three switching transistors.

# Note: All signals (a, b, c, d, e, f, g, dot, enable 1, enable 2, enable 3) used for controlling 7-Segment display are active-low signals. So, for example, for displaying “8” in display-2, users need to drive Enable 2 to 0 as well as drive signals a, b, c, d, e, f to 0. All other signals need to be driven to 1.

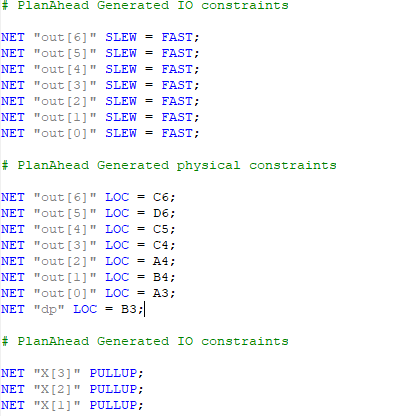


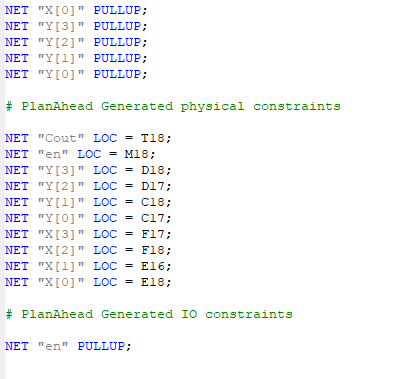
**Code:**





**UCF File:**





**I/O Pin Planning:**

